IN THE CLAIMS

Please cancel claims 1-20 without disclaimer or prejudice to be pursued in this or a later-filed continuation or continuation-in-part application.

Please add the following new claims.

1-24. (canceled)

25. (new) A method for generating test patterns for testing logic products on a test system, comprising:

generating an initial sequence of test vectors having a plurality of bits comprising care bits and non-care bits;

forming a set of filled test vectors by:

for a selected test vector in said initial sequence, filling said non-care bits of said selected test vector with preselected values; and

for each subsequent test vector in said initial sequence, filling each of said non-care bits of said subsequent test vector with a value of an associated bit of a preceding test vector immediately preceding said subsequent test vector in said initial sequence;

removing at least one redundant test vector from said filled test vectors to form a minimum set of said filled test vectors;

compressing said minimum set of said filled test vectors to form a compressed vector data set;

transmitting said compressed vector data set to the test system along with restoration information for restoring said at least one redundant test vector;

recovering said care bits of said test vectors in said initial sequence from said compressed vector data set in accordance with said restoration information; and

loading said care bits recovered from said compressed vector data set into input latches of the test system.

26. (new) The method of claim 25, wherein said filling said non-care bits of said selected test vector comprises filling said non-care bits of a first test vector in said initial sequence with preselected values.

27. (new) The method of claim 25, wherein said filling said non-care bits of said selected test vector comprises filling each of said non-care bits of said selected test vector with a uniform preselected value.

28. (new) The method of claim 27, wherein said filling said non-care bits of said selected test vector comprises filling each of said non-care bits of said selected test vector with a "0".

29. (new) The method of claim 25, wherein said filling said non-care bits of said selected test vector comprises filling said non-care bits of said selected test vector with a random distribution of values of both "0" and "1".

30. (new) The method of claim 25, wherein said recovering said care bits of said test vectors in said initial sequence includes:

decompressing said compressed vector data set to recover said minimum set of said filled test vectors; and

restoring said at least one redundant test vector to said minimum set of said filled test vectors in accordance with said restoration information to recover said filled test vectors.